Design and Implementation of BCD Adder and Subtractor using Reversible Gates

Amita Mishra* and Mr. Manish Saxena**
*M.Tech scholar, Department of ECE, BIST Bhopal, India
amitam54@gmail.com
**Assistant Professor, Department of ECE, BIST Bhopal, India
manish.saxena2008@gmail.com

Abstract: Programmable reversible logic is emerging as a prospective logic design style for implementation in modern nanotechnology and quantum computing with minimal impact on circuit heat generation. Recent advances in reversible logic using and quantum computer algorithms allow for improved computer architecture and arithmetic logic unit designs. Arithmetic unit design using reversible logic gate has received much attention as it reduces power dissipation with no loss of information. This paper proposes the design of 32-bit Binary Coded Decimal (BCD) addition and subtraction unit using reversible logic gates. The reversible 32 -bit BCD addition unit is designed using the following modules such as reversible 4-bit Carry Propagate unit using reversible logic gates such as Feynman gate and URG gate and a reversible 4-bit error correction unit. The 4-bit error correcting unit designed by reversible (4x1) Multiplexer (MUX) unit using Toffoli gate and TNOR gates to provide the output with a precise value. The reversible 32-bit BCD subtraction unit is designed based on the nine's complement method of 4-bit reversible BCD addition. The proposed design is synthesized using Xilinx ISE software and simulated using VHDL test bench.

Keywords: Reversible Gates, Adder/ Sub tractor, Garbage Output, Quantum Cost.

Introduction

In modern VLSI system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with each year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design.

Reversible logic has its basics from thermodynamics of information processing. According to this, traditional irreversible circuits generate heat due to the loss of information during computation. In order to avoid this information loss the conventional circuits are modeled using reversible logic. Landauer[1961]showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits [1]. It is proved that the loss of one bit of information results in dissipation of KT*log2 joules of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed. Benett [1973] showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates [2]. A gate is considered to be reversible only if for each and every input there is a unique output assignment. Hence there is a one to one mapping between the input and output vectors. A reversible logic gate is an n –input, n- output device indicating that it has same number of inputs and outputs. A circuit that is built from reversible gates is known as reversible logic circuit. In this paper, we design a 16 bit reversible ALU that can perform eight operations simultaneously. The eight operations include addition, subtraction, AND, NAND, OR, NOR and XOR. All the modules are simulated in modalism SE 6.5 and synthesized using Xilinx ISE 14.1. Reversible logic is gaining importance in areas of CMOS design because of its low power dissipation. The traditional gates like AND, OR, XOR are all irreversible gates. Consider the case of traditional AND gate. It consists of two inputs and one output. As a result, one bit is lost each time a computation is carried out. According to the truth table shown in Fig.1, there are three inputs (1, 0), (0, 1) and (0, 0) that corresponds to an output zero. Hence it is not possible to determine a unique input that resulted in the output zero. In order to make a gate reversible additional input and output lines are added so that a one to one mapping exists between the input and output. This prevents the loss of information that is main cause of power dissipation in irreversible circuits. The input that is added to an m x n function to make it reversible is known as constant input (CI). All the outputs of a reversible circuit need not be used in the circuit. Those outputs that are not used in the circuit is called as garbage output (GO). The number of garbage output for a particular reversible gate is not fixed. The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

Litrature Survey

Ms. A. Anjana et al. [1], Arithmetic unit design using reversible logic gate has received much attention as it reduces power dissipation with no loss of information. This paper proposes the design of 32-bit Binary Coded Decimal (BCD) addition and subtraction unit using reversible logic gates. The reversible 32 -bit BCD addition unit is designed using the following modules such as reversible 4-bit Carry Propagate unit using reversible logic gates such as Feynman gate and URG gate and a reversible 4-bit error correction unit. The 4-bit error correcting unit designed by reversible (4x1) Multiplexer (MUX) unit using Toffoli gate and TNOR gates to provide the output with a precise BCD value. The reversible 32-bit BCD subtraction unit is designed based on the nine's complement method of 4-bit reversible BCD addition. In BCD subtraction unit, the error correcting block is designed with the conditional reversible logic COG gate to make the necessary corrections at the output to get exact output. The reversible 32- bit BCD addition and subtraction unit is designed based on the parallel pipelined unit to enhance the speed of operation. This proposed reversible 32-bit BCD addition module has 416 garbage BCD values with the critical path delay of 17.420 ns; reversible 32-bit BCD subtraction module has 240 garbage BCD values with the critical path delay of about 17.420 ns.

Matthew Morrison et al [2], proposed the outline of two programmable reversible rationale door structures focused at BCD execution and their utilization in the acknowledgment of a productive reversible BCD is illustrated. The proposed BCD configuration is checked and its points of interest over the main existing BCD outline are quantitatively analyzed. Reversible rationale is generally being considered as the potential rationale configuration style for usage in present day nanotechnology and quantum figuring with negligibleeffect on physical entropy. Late advances in reversible rationale take into account enhanced quantum PC calculations and plans for comparing PC architectures. Huge commitments have been made in the writing towards the configuration of reversible rationale door structures and number-crunching units, nonetheless, there are very few endeavors coordinated towards the outline of reversible BCDs. They propose the outline of two programmable reversible rationaledoor structures focused at BCD execution and their utilization in the acknowledgment of a proficient reversible BCD is illustrated. The proposed BCD configuration is confirmed and its preferences over the main existing BCD outline are quantitatively investigated.

Lekshmi Viswanath et al [3], reversible or information-lossless circuits have applications in digital signal processing, communication, computer graphics and cryptography. Reversibility plays an important role when energy efficient computations are considered. Reversible logic is used to reduce the power dissipation that occurs in classical circuits by preventing the loss of information. They propose a reversible design of a 16 bit BCD. This BCD consists of eight operations, three arithmetic and five logical operations. The arithmetic operations include addition, subtraction, multiplication and the logical operations include NAND, AND, OR, NOT and XOR. All the modules are being designed using the basic reversible gates. The power and delay analysis of the various sub modules is performed and a comparison with the traditional circuits is also carried out.

Akanksha Dixit et al [4], reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications in advanced computing, low power design, Optical information processing,. Conventional digital circuits dissipate a significant amount of energy because bits of information are erased during the logic operations. Thus, if logic gates are designed such that the information bits are not destroyed, the power consumption can be reduced dramatically. The information bits are not lost in case of a reversible computation. This has led to the development of reversible gates. BCD is a fundamental building block of a central processing unit (CPU) in any computing system; reversible arithmetic unit has a high power optimization on the offer. By using suitable control logic to one of the input variables of parallel adder, various arithmetic operations can be realized.

Tat Ngai et al [5], the proposed BCD configuration is checked and its points of interest over the main existing BCD outline are quantitatively analyzed. Reversible rationale is generally being considered as the potential rationale configuration style for usage in present day nanotechnology and quantum figuring with negligible effect on physical entropy. Late advances in reversible rationale take into account enhanced quantum PC calculations and plans for comparing PC architectures. Huge commitments have been made in the writing towards the configuration of reversible rationale door structures and number-crunching units, nonetheless, there are very few endeavors coordinated towards the outline of reversible BCDs. The outline of two programmable reversible rationale door structures focused at BCD execution and their utilization in the acknowledgment of a proficient reversible BCD is illustrated. The proposed BCD configuration is confirmed and its preferences over the main existing BCD outline are quantitatively investigated.

Kazuo Sakiyama et al. [6], huge commitments have been made in the writing towards the configuration of reversible rationale door structures and number-crunching units, nonetheless, there are very few endeavors coordinated towards the outline of reversible BCDs. They propose the outline of two programmable reversible rationale door structures focused at BCD execution and their utilization in the acknowledgment of a proficient reversible BCD is illustrated. The proposed BCD configuration is confirmed and its preferences over the main existing BCD outline are quantitatively investigated. Thus, if logic gates are designed such that the information bits are not destroyed, the power consumption can be reduced dramatically. The information bits are not lost in case of a reversible computation. This has led to the development of reversible gates. BCD is a fundamental building block of a central processing unit (CPU) in any computing system; reversible arithmetic unit has a high power optimization on the offer. By using suitable control logic to one of the input variables of parallel adder, various arithmetic operations can be realized. BCD based on a Reversible low power control unit for arithmetic & logic operations is proposed. In our design, the full Adders are realized using synthesizable, low quantum cost, low garbage output Peres gates. This paper presents a novel design of Arithmetic & Logical Unit using Reversible control unit. This Reversible BCD has been modeled and verified using Verilog and Quartus II 5.0 simulator. Comparative results are presented in terms of number of gates, number of garbage outputs, number of constant inputs and Quantum cost.

Vivechana Dubey et al. [7], this paper deals with Thermal Analysis of Energy Efficient Clock Gated Arithmetic Logic Unit on FPGA for reduction of leakage power and total power consumption and it has been analyzed that there is reduction in Leakage Power when ambient temperature decreases from 50 degree Celsius to 20 degree Celsius. Virtex-6 is 40-nm FPGA, on which Thermal Analysis of Energy Efficient Clock Gated Arithmetic Logic Unit has been analyzed with device operating frequency is 1GHz. This reduction in leakage power is analyzed on arithmetic and logic unit with latch free clock gating technique and on arithmetic and logic unit with latch based clock gating technique. There is significant Leakage power reduction by varying ambient temperature. With Latch free clock gating technique in Low Power Arithmetic and Logic Unit the Contribution of leakage power was 1.327W, when Ambient Temperature is 50 degree Celsius, which is further reduced to 1.246W at 40 degree Celsius Ambient Temperature, 1.176W at 30 degree Celsius Ambient Temperature, 1.114W at 20 degree Celsius Ambient Temperature. With Latch based clock gating technique in Low Power Arithmetic and Logic Unit the Contribution of leakage power was 1.328W When Ambient Temperature is 50 degree Celsius, which is further reduced to 1.247W at 40 degree Celsius Ambient Temperature, 1.177W at 30 degree Celsius Ambient Temperature, 1.115W at 30 degree Celsius AmbientTemperature. So, there is reduction in leakage power in energy efficient arithmetic and logic unit.

Abhishek Gupta et al. [8], this has led to the development of reversible gates. BCD is a fundamental building block of a central processing unit (CPU) in any computing system; reversible arithmetic unit has a high power optimization on the offer. By using suitable control logic to one of the input variables of parallel adder, various arithmetic operations can be realized. BCD based on a Reversible low power control unit for arithmetic & logic operations is proposed. In our design, the full Adders are realized using synthesizable, low quantum cost, low garbage output Peres gates. This paper presents a novel design of Arithmetic & Logical Unit using Reversible control unit. This Reversible BCD has been modeled and verified using Verilog and Quartus II 5.0 simulator. Comparative results are presented in terms of number of gates, number of garbage outputs, number of constant inputs and Quantum cost.

Nidhi Gupta et al [9], After an intensive study and profound investigation they have found that Vedic Urdhva Triyambakam duplication calculation is the best calculation as it produces partial products in the parallel way. They proposed another tree augmentation structure based construction modeling to plan this Vedic multiplier. To create mostly created items gap and conquer approach has been utilized. For the expansion of halfway created items another expansion tree structure has been proposed. It provides better speed in correlation Array, Booth, Wallace, Modified Booth Wallace, Karatsuba and Vedic Karatsuba Multiplier and additionally it is faster than Vedic multiplier which has been proposed by L. Shriraman and Devika Jaina.
In order to make BCD's vitality and force effective, once again reversible rationale entryway has been proposed which is like Fredkin Gate. In the wake up of combining these modules they have picked up the vitality, velocity, and force effective BCD's for their designs.

Reversible Gates

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gate available. It is most commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize the various Boolean functions in various logical architectures.

Table 1: Summary of Literature Review

Entitle of paper	Approached used	Software	Parameter	Published Year
Design of Reversible 32-Bit BCD Add-Subtract Unit using Parallel Pipelined Method	Design 32-bit BCD adder using reversible gate	Xilinx 12.1	LUTs = 90, IOBs= 98, delay 17.420 ns	IEEE 2016
Design of a Reversible ALU based on Novel Programmable Reversible Logic Gate Structures	Design ALU using reversible gate	Xilinx 12.1	LUTs = 100, IOBs= 98, delay 19.520 ns	IEEE 2015
Design and Analysis of 16 Bit Reversible ALU	Design 16-bit ALU using reversible gate	Xilinx ISE 12.2	LUTs = 121, IOBs= 98, delay 21.420 ns	IEEE 2014
Arithmetic & Logic Unit (ALU) Design using Reversible Control Unit	ALU using Reversible Control Unit	Xilinx 9.1	LUTs = 132, IOBs= 98, delay 27.620 ns	IEEE 2014
Enhanced Concurrent Error Correcting Arithmetic Unit Design Using Alternating Logic	ALU using Reversible Control Unit	Xilinx 9.1	LUTs = 152, IOBs= 104, delay 29.720 ns	IEEE 2001
A Fast Dual-Field Modular Arithmetic Logic Unit and ItsHardware Implementation	modular using Reversible Control	Xilinx 8.1	LUTs = 132, IOBs= 98, delay 27.620 ns	IEEE 2006
An Arithmetic and Logic Unit Optimized for Area and power	Arithmetic using Reversible Control	Xilinx 8.1	LUTs = 142, IOBs= 128, delay 30.820 ns	IEEE 2014
Design of Speed, Energy and Power Efficient Reversible Logic Based Vedic ALU for Digital Processors	ALU using Reversible Control Unit	Xilinx 7.1	LUTs = 172, IOBs= 188, delay 33.020 ns	IEEE 2012
Thermal Analysis of Energy Efficient Clock Gated Arithmetic Logic Unit on FPGA	Thermal analysis using Reversible Control Unit	Xilinx 6.2	LUTs = 152, IOBs= 198, delay 37.620 ns	IEEE 2014

Basic Reversible Gates

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

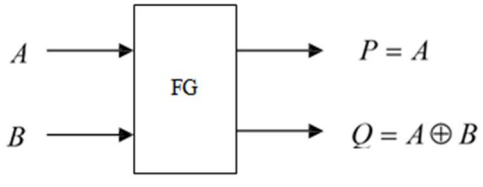

Figure 1: Feynman gate

In figure 2, the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

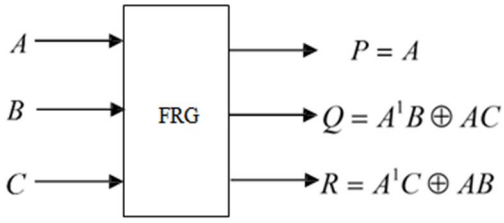

Figure 2: Fredkin gate

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstandingthe fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

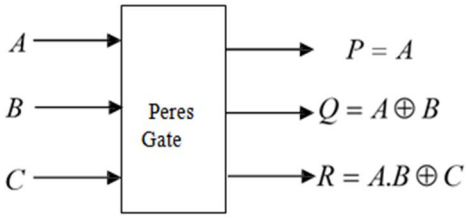

Figure 3: Peres gate

The HNG gate, presented in fig, produces the following logical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 4.

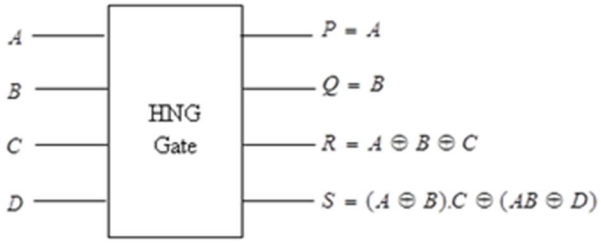

Figure 4: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure- Peres And-Or (PAOG) gate – is presented which produces outputs

$$P = A \quad (5)$$

$$Q = A \oplus B \quad (6)$$

$$R = AB \oplus C \quad (7)$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \quad (8)$$

Fig. 5 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

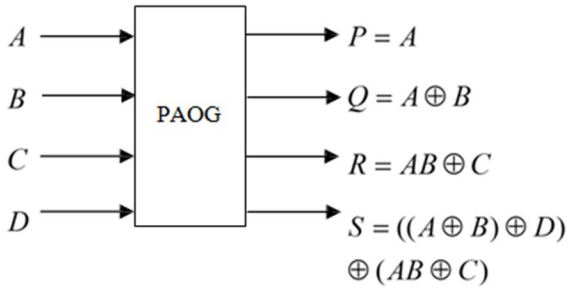

Figure 5: Block Diagram of the PAOG

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DKG gate produces the following logical output calculations:

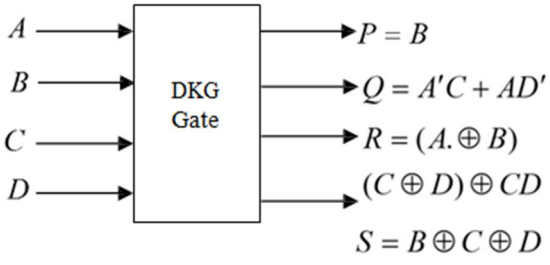

Figure 6: DKG Gate

$$P = B \tag{9}$$

$$Q = A'C + AD' \tag{10}$$

$$R = (A. \oplus B)(C \oplus D) \oplus CD \tag{11}$$

$$S = B \oplus C \oplus D \tag{12}$$

Proposed Methodology

In this paper, reversible logic gates are used to realize the 32-bit BCD addition and subtraction units. Reversible logic gates are employed so as to reduce the delay and power dissipation in the BCD arithmetic unit. BCD adder adds two input data and produces the sum as the result. On account of any error in the sum value like the output data so generated is not a BCD number then there needs a correction block for the error output so produced [7]. Reversible BCD subtraction unit subtracts the two input values and generates the difference value as the output. In the proposed design, subtraction is realized by taking the nine's complement and adding the complemented value along with the other input data [8].

Reversible 32-bit BCD addition unit is realized by cascading eight 4- bit BCD adder along with the error correction unit designed individually in the Carry Propagate adder (CPA) fashion. Reversible logic gates used in this designing are Feynman gate and URG gate for about 4-bit input vectors.

Figure 7 shows the block diagram of the 1-bit full subtract or. In this diagram used one ancilla input and two garbage outputs. 1-bit full subtractor design of the two TR gate is connected to the series i.e. the output of the first TR gate is connected to the input of the second. It is found that the 1-bit full subtractor used in two reversible TR gate. Maximum delay count of the 1- bit subtractor is 10 and quantum cost of the circuit is 12.

Figure 8 shows the n-bit full subtractor using TR gate. It is clearly that carry of the 1-bit TR gate is connected to the 2-bit TR gate. TR gate consist of three inputs and three outputs. TR gate like as a half subtractor it is assume the third bit zero.

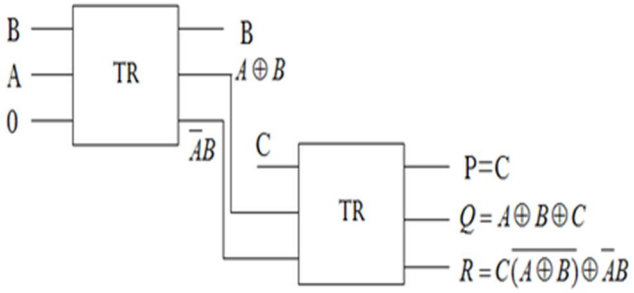

Figure 7: Block Diagram of 1-bit Full Sub tractor

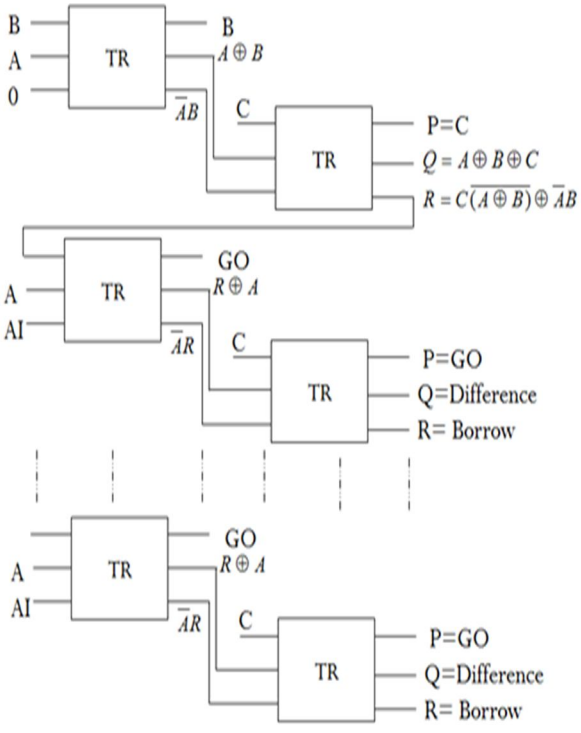

Figure 8: Block Diagram of n-bit Full Sub tractor

Figure 9 shows the block diagram of the 1-bit full adder. In this diagram used one ancilla input and two garbage outputs. 1-bit full adder design of the two Peres gate is connected to the series i.e. the output of the first Peres gate is connected to the input of the second. It is found that the 1-bit full adder used in two reversible Peres gate. Maximum delay count of the 1-bit adder is 10 and quantum cost of the circuit is 12.

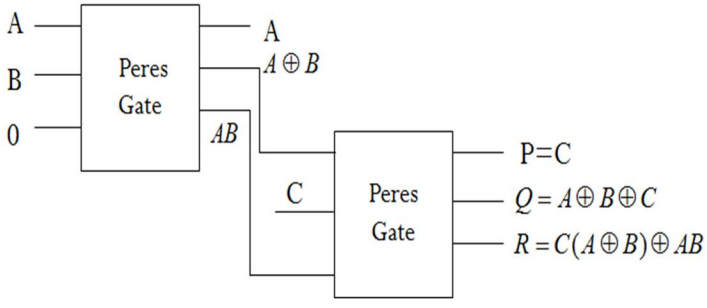

Figure 9: Block Diagram of 1-bit Full Adder

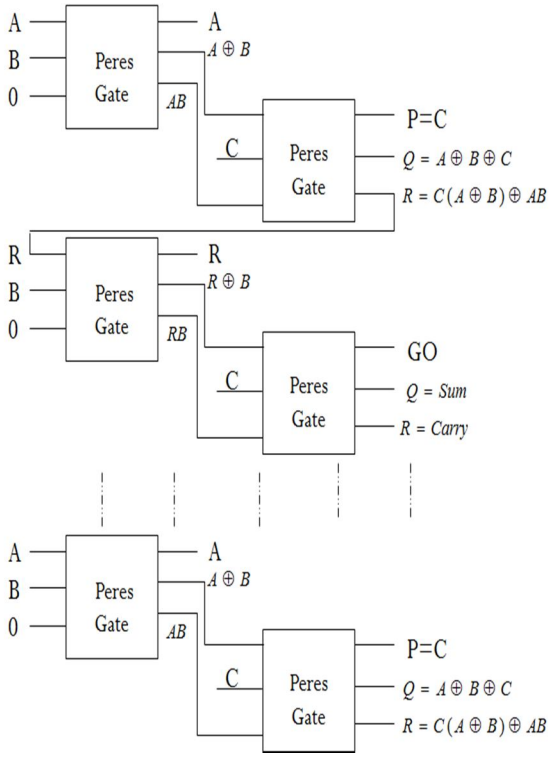

Figure 10: Block Diagram of n-bit Full Adder

Simulation Result

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 6.2i updated version. Xilinx 6.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISETM (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 6.2i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to design solution.
We are using Peres Gate and DKG Gate as a result of whichno. of slice look up tables, no of bounded IOBs will reduced and delay will also get reduced by few nano seconds.

Conclusion

The 4bit, 8bit, 16bit and 32bit Adder/ Sub tractor is designed by integrating various sub modules that includes DKG logic Gate. The performance evaluation of the various sub modules are carried out using Xilinx 14.1 ISE Simulator and it was found that the circuits designed using reversible logic showed a reduced delay and power. As a future work more arithmetic and logical function can be used.

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